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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,065	11/18/2003	Paige Bushner	14538US02	4795

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EXAMINER	
LE, NHAN T	

ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/716,065	BUSHNER, PAIGE	
	Examiner	Art Unit	
	Nhan T. Le	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 2, 3, 8-11, 14, 15, 19-20, 31-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirata et al (2002/0059651).

As to claims 1, 31, 42, Hirata teaches a system for an integrated set-top box, the system comprising: a single integrated circuit chip comprising: a first satellite receiver demodulator (see fig. 2b, 2a, 3a, paragraphs 0060-0062) integrated within the single integrated circuit chip; at least a second satellite receiver demodulator (see fig. 2b, 2b, 3b, paragraphs 0060-0062) integrated within the single integrated circuit chip; and at least one processor (see fig. 2b, 4, paragraphs 0060-0062) integrated within the single integrated circuit chip and coupled to the first satellite receiver demodulator and the second satellite receiver demodulator.

As to claim 2, Hirata teaches wherein the at least one processor comprises at least one data transport processor (see paragraph 0062).

As to claims 3, 8, Hirata teaches a programmable memory integrated within the single integrated circuit chip (see paragraph 0062); wherein the programmable memory is a one-time programmable memory (see paragraph 0062).

As to claims 9, 32, Hirata teaches at least one video decoder integrated within the single integrated circuit chip and coupled to the at least one processor (see paragraph 0013).

As to claim 10, Hirata teaches wherein the at least one video decoder is a standard definition MPEG-2 video decoder (see paragraph 0069).

As to claims 11, 33, 34, 37, 38, 39, Hirata teaches at least one video and graphics display engine integrated within the single integrated circuit chip and coupled to the at least one video decoder (see paragraph 0062).

As to claims 14, 15, 35, 36, 40, 41, Hirata teaches at least one audio decoder integrated within the single integrated circuit chip and coupled to the at least one processor, wherein the at least one audio decoder is an MPEG-2 audio decoder (see paragraph 0003).

As to claim 19, Hirata teaches a digital satellite equipment control bus integrated within the single integrated circuit chip (see paragraph 0012).

As to claim 20, Hirata teaches at least one of a plurality of peripheral interfaces comprising a serial peripheral interface, general purpose input/output pins, integrated within the single integrated circuit chip (see paragraphs 0080-0083).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata et al (2002/0059651) in view of Dorenbosch et al (US 6,256,493).

As to claims 4-6, Hirata fails to teach wherein the programmable memory stores at least one of security information and configuration information for the single integrated circuit chip; wherein the security information comprises at least one of a security key and a device identifier (ID); wherein the device identifier comprises at least one of an electronic serial number and an address. Dorenbosch teaches wherein the programmable memory stores at least one of security information and configuration information for the single integrated circuit chip; wherein the security information comprises at least one of a security key and a device identifier (ID); wherein the device identifier comprises at least one of an electronic serial number and an address (see col. 4, lines 1-50). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Dorenbosch into the system of Hirata in order to prevent unauthorized access to the device.

3. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata et al (2002/0059651) in view of Dorenbosch et al (US 6,256,493) further in view of Hendrickson et al (US 5, 384,847).

As to claim 7, the combination of hirata and Dorenbosch fails to teach wherein the configuration information comprises at least one of configuration data and code for configuring the single integrated circuit chip. Hendrickson teaches wherein the configuration information comprises at least one of configuration data and code for configuring the single integrated circuit chip (see col. 10, lines 22-39). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Hendickson into the system of Hirata and Dorenbosch in order to provide the higher level of security for the system.

4. Claims 12, 13, 16-18, 21-27, 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata et al (2002/0059651) in view of Middeke et al (US 6,445,907).

As to claims 12, 13, Hirata fails to teach at least one video encoder integrated within the single integrated circuit chip and coupled to the at least one video and graphics display engine; at least one video digital-to-analog converter and RF modulator integrated within the single integrated circuit chip and coupled to the at least one video encoder. Middeke teaches at least one video encoder integrated within the single integrated circuit chip and coupled to the at least one video and graphics display engine; at least one video digital-to-analog converter and RF modulator integrated within the single integrated circuit chip and coupled to the at least one video encoder (see fig. 2, numbers 52, RF, col. 4, lines 25-39). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Middeke into the system of Hirata in order to analyze the received signals.

As to claim 16, the combination of Hirata and Middeke teaches at least one audio digital-to-analog converter integrated within the single integrated circuit chip and coupled to the at least one audio decoder (see Middeke fig. 2, numbers 54, RF, col. 4, lines 25-39).

As to claims 17, 18, the combination of Hirata and Middeke teaches at least one memory controller integrated within the single integrated circuit chip and coupled to at least the at least one processor; wherein the at least one memory controller comprises a DRAM memory controller (see Middeke fig. 2, numbers 54, RF, col. 4, lines 4, 25-39).

As to claims 21, 22, the combination of Hirata and Middeke teaches at least one read-only memory integrated within the single integrated circuit chip; wherein the at least one read-only memory comprises a CPU boot ROM and a FLASH (see Middeke col. 4, lines 25-39, col. 5, lines 60-67).

As to claims 23, 24, the combination of Hirata and Middeke teaches at least one debug port integrated within the single integrated circuit chip, wherein the debug port comprises a JTAG port or any variation thereof (see Middeke col. 4, lines 25-39).

As to claims 25, 26, the combination of Hirata and Middeke teaches at least one card reader integrated within the single integrated circuit chip, wherein the card reader is a smart card reader (see Middeke col. 4, lines 25-39).

As to claim 27, the combination of Hirata and Middeke teaches one voltage regulator integrated within the single integrated circuit chip (see Middeke col. 6, lines 56-67).

As to claim 29, the combination of Hirata and Middeke teaches one telephony modem integrated within the single integrated circuit chip (see Middeke col. 6, lines 56-67).

As to claim 30, the combination of Hirata and Middeke teaches wherein the first satellite receiver demodulator and the second satellite receiver demodulator are at least one of QPSK demodulators (see Middeke col. 4, lines 25-39, col. 7, lines 26-42).

5. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata et al (2002/0059651) in view of Bauer (US 2001/0024962).

As to claim 28, Hirata fails to teach one phase lock loop integrated within the single integrated circuit chip. Bauer teaches one phase lock loop integrated within the single integrated circuit chip (see paragraph 017). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Bauer into the system of Hirata in order to control the frequency in the IC system.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Le whose telephone number is 571-272-7892. The examiner can normally be reached on 08:00-05:00 (Mon-Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on 571-272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

N. Le

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